Network Equivalence of Port Discontinuity Related to Source Plane in a Deterministic 3-D Method of Moments

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***Abstract*— Port discontinuity in a deterministic three-dimensional (3-D) method of moments (MoM) algorithm using the impressed voltage excitation is accurately modeled in terms of its equivalent circuit network. This is done through the application of a newly developed scheme called the short-open calibration (SOC) technique. The resulting network equivalence can be explicitly formulated by the use of an analytical procedure. It is observed from our predicted results that the port discontinuity can be reasonably equivalent to a lumped shunt capacitance at low frequency while at high frequency it should be modeled as a dispersive circuit network.**

***Index Terms*—Method of moments, port discontinuity.**

I. INTRODUCTION

THE deterministic three-dimensional (3-D) method of moments (MoM) using the impressed voltage excitation has been well developed and widely used as a powerful tool for modeling multilayered planar circuits and antennas having arbitrarily shaped geometry [1]–[3]. As dictated by its technical feature, this type of MoM algorithm is more suited to the handling of electrically large problems such as resonator antenna and filter. It is found, however, that they are relatively inaccurate in the characterization of electrically small structures in terms of their equivalent circuits defined at the reference planes of interest, such as the two open-ends of gap discontinuities. This is largely attributed to the intrinsic unwanted parasitic effects essentially brought by the approximation of impressed voltage excitation scheme [4]. Even though very small, these effects are rather harmful for accurate parameter extraction because they are comparable with the circuit parameters themselves, thereby leading to significant error in the network equivalence translated from the modeling results [4]. In addition, they are usually frequency and dimension dependent.

This issue has been rarely addressed in relation to the port discontinuity effect and its circuit representation in the MoM algorithm, except in the approximate models proposed in [4] and [5]. Under the assumption of a shielded structure, Rautio [4] considered the port discontinuity simply as a purely shunt capacitance and characterized it by applying two standards, namely, through and double-length through lines. On the other hand, a series impedance was introduced into the port discontinuity [5] to provide an additional degree of freedom. By analog to a through-reflect-line (TRL) scheme used in the microwave measurement [6], a newly proposed short-open calibration (SOC) technique [8], [9] was presented in a deterministic 3-D MoM algorithm [7] for modeling unbounded discontinuities in terms of their equivalent circuit network. In this letter, this SOC technique is applied to modeling of the port discontinuity as a generalized equivalent circuit network without resorting to any preassumption.

II. FORMULATION

The port discontinuity was introduced by the approximation of the impressed voltage excitation [2]–[4] in a deterministic 3-D MoM algorithm [1]–[3], [7]. An SOC technique [8], [9] is applied here for its electrical characterization. Fig. 1 shows the physical model of the port discontinuity and its equivalent network. In Fig. 1(a), an electrically long microstrip line is divided into two distinct parts: two feed lines and a uniform line. In addition, the two feed lines are simultaneously driven by a pair of impressed voltages backed by local electrical wall V_1 and V_2 at ports denoted as #1 and #2, while the uniform line located between two reference planes #1′ and #2′ is kept electrically far away from the two local electrical walls. To simplify the problem, all the three lines are equal in length. The equivalent network is schematically described in Fig. 1(b) where the uniform line is generally considered as a lossy and dispersive transmission line. The two feed lines are arranged by cascaded line as well as admittance circuit that characterizes the port discontinuity.

With the MoM algorithm described in [7], the two feed lines and uniform line are separately modeled by using appropriate Green's functions. The electric walls of the two source planes are removed by applying an image principle so that an unbounded environment can be effectively simulated. Using a Galerkin's technique, a source-type matrix equation can easily be formulated for the explicit representation of a relationship between the equivalent currents and voltages $I_1,\ I_2,\ V_1,\ V_2$ at the two planes #1 and #2. The relationship can be simply described by an equivalent $ABCD$ matrix $[A]$ in terms of chain matrices $[A^f]$ and $[A^l]$, in connection with the two feed lines and uniform line, such as

$$[A] = [A^f]\cdot[A^l]\cdot\{[U]\cdot[A^f]\cdot[U]\}^{-1} \qquad (1)$$

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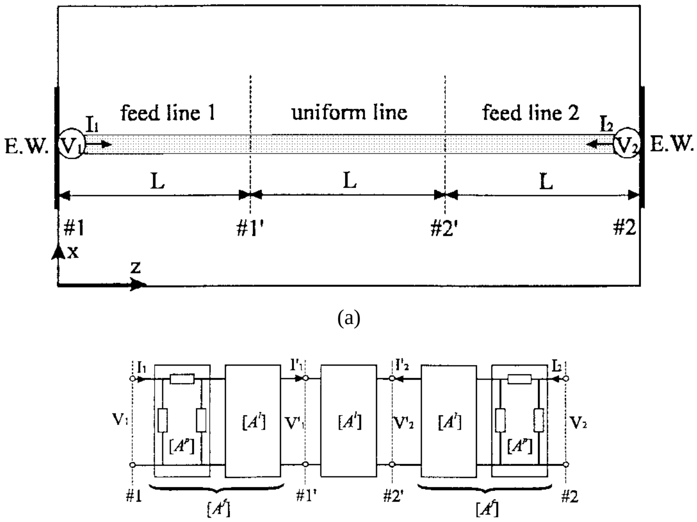

Fig. 1. Electrical characterization of port discontinuity in a deterministic method of moments. (a) Physical model. (b) Equivalent circuit network.

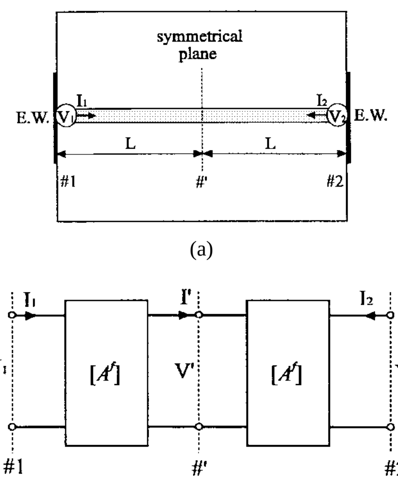

Fig. 2. Physical model and its equivalent network of a symmetrical microstrip line in formulating the two standard elements (short and open) for the proposed SOC technique. (a) Physical model. (b) Equivalent network.

where $[U]$ is a sign matrix with elements: $U_{11} = 1, U_{22} = -1$, and $U_{12} = U_{21} = 0$. Subsequently, two standards [8], [9], namely short and open, are formulated by a symmetrical line having the length of twice the feed line, respectively, driven by a pair of odd/even excitations at its two ports as shown in Fig. 2(a). This is to say, the feed lines and uniform line are completely equivalent to the error boxes and the device under test (DUT) as in the TRL scheme. All the equivalent electric currents, I_1, I_2, and I' flowing at the two ports and symmetrical plane can be analytically expressed as a function of the two-port voltages so that the matrix related to the error box $[A^f]$ can be numerically obtained under the MoM algorithm. Thereafter, $[A^f]$ is cast into (1) and thus the $ABCD$ matrix related to the uniform line $[A^l]$ is easily formulated in terms of $[A]$ and $[A^f]$.

In addition, each feed line consists of two separate parts: the port discontinuity and a segment of uniform line, which are characterized by the admittance matrix and equivalent transmission line matrix as indicated in Fig. 1(b). Since all of the parasitic effects brought by the existence of an impressed voltage backed by an electric wall are completely taken into account in the port discontinuity, the transmission line is physically identical to the uniform line connecting the two feed lines. As a result, the port discontinuity $[A^p]$ can be extracted by the two numerically evaluated matrices $[A]$ and $[A^f]$ in the above-described two-step algorithm. It is easy to find that

$$[A^p] = [A^f] \cdot \{[A] \cdot [U] \cdot [A^f] \cdot [U]\}^{-1} \cdot [A^f]. \qquad (2)$$

III. Results and Discussion

Equation (2) suggests that the port discontinuity be effectively represented by a dynamic network equivalence which generally includes all of potential physical effects such as frequency dispersion, high-order modes effect, and radiation/leakage loss for unbounded cases. In line with the discussion of [4] and [5] for a shielded case, only the lossless elements in the $ABCD$ matrix for the port discontinuity are considered in this work to facilitate our following discussion.

Fig. 3 shows a set of simulated curves of four matrix elements defined by (2) in the frequency range from 1 to 20 GHz. Three groups of curves for different length L, corresponding to the mesh number $N_L = 15, 20$, and 25, are respectively, calculated and plotted together to confirm the numerical stability and accuracy of our algorithm. In Fig. 3(a), it can be clearly seen that the diagonal elements A and D remain a unit value at frequency below 6 GHz, confirming the suitability and validity of the assumption made in [4], that is $A = D = 1$, while they tend to be varied in the high-frequency range with a change smaller than 1.2% $(N_L = 15)$, 1.0% $(N_L = 20)$, and 0.5% $(N_L = 25)$, respectively. In Fig. 3(b), the element C appears to be linear with frequency in the entire frequency range of interest, indicating very well that the lumped shunt capacitance is indeed valid as predicted in [4], while the element B shows a visible value at frequency below 6 GHz, representing a series impedance as described in [5], and it appears to be randomly changed with frequency (f) and length of choice (N_L) as frequency goes beyond 6 GHz. Due to the fact that there is no report available relating to this issue, such a randomness, in our opinion, is mainly caused by numerical error (noise) accompanied in the extraction of lumped circuit network from calculated parameters using the MoM algorithm.

Judging from these facts, the port discontinuity in the MoM algorithm can be adequately modeled as a purely shunt capacitor and a series impedance at operating frequency below 6 GHz. Fig. 4 provides a close look at three groups of simulated curves related to the equivalent capacitance $C_e = C/\omega$ and inductance $L_e = B/\omega$ as a function of the strip width of a microstrip line for three different low frequencies $f = 1, 3$, and 5 GHz. It is more pronounced from Fig. 4 that the port discontinuity can be regarded actually as a simplified circuit network with only the shunt capacitor under such limiting conditions as in the consideration of an extremely low frequency or very narrow strip width. As the strip width increases, the term C_e always appears invariantly linear with

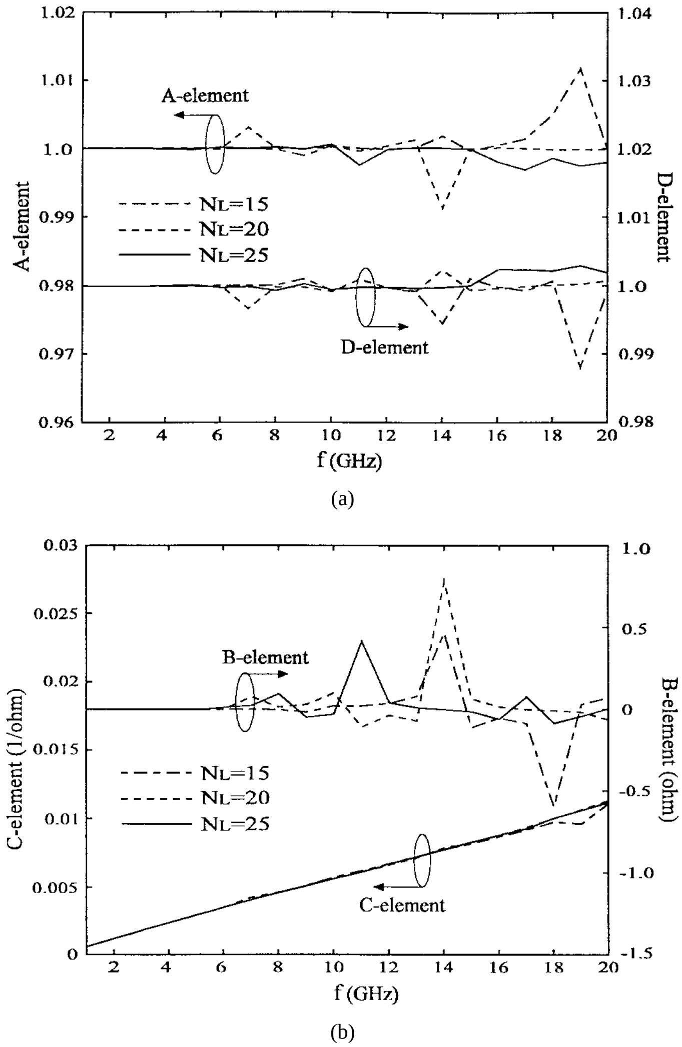

Fig. 3. Simulated curves showing frequency-dependent $ABCD$ elements for different length of the microstrip line ($\varepsilon_r = 9.7, w = h = 0.635$ mm, mesh size: $\Delta x = 0.127$ mm, $\Delta z = 0.3175$ mm). (a) Elements A and D. (b) Elements B and C.

the strip width regardless of frequency while the term L_e tends to be very sensitive to frequency. Therefore, Figs. 3 and 4 suggest that the assumption of the lumped circuit model proposed in [2] and [3] is reasonably accurate for modeling microstrip discontinuities in the case of electrically thin substrate and electrically narrow strip width of feed line.

IV. Conclusion

The port discontinuity introduced at the source plane in a deterministic 3-D method of moments using the impressed voltage excitation is accurately modeled as an equivalent circuit network through the application of a newly proposed SOC technique. The simulated results show that the equivalent network can be described simply by a lumped shunt capacitance at low frequency as predicted in [4] while it

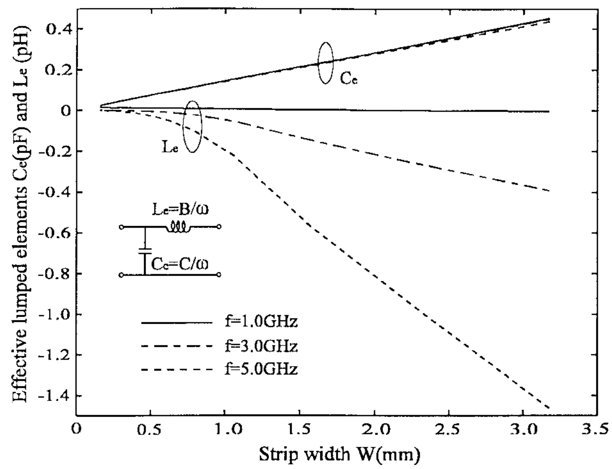

Fig. 4. Electrical behavior of the equivalent shunt capacitance C_e and series inductance L_e as a function of the strip width at low frequency under the same physical conditions as in Fig. 3.

should be otherwise considered as a dispersive network at high frequency. In addition, it is indicated that such a technique can be very accurate and effective in modeling microstrip discontinuities considering a large variety of physical effects.

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